DO NOT ENTER TM 11/07/05

IN THE CLAIMS:

Claims 1 and 10 are amended herein. Please cancel claims 19-27 without prejudice or disclaimer. All pending claims and their present status are produced below.

1. (Currently amended) A method for performing arithmetic in a memory to memory architecture in an embedded processor, the method comprising:

receiving a 32-bit fixed length instruction, the instruction specifying a source address in a memory using 11 bits, a source address in a register file using 5 bits, a destination address in the memory using 11 bits, and a mathematical operation to be performed using 5 bits; and

responsive to receiving the fixed length instruction:

accessing, from the source address in the memory, a first operand on which the mathematical operation is to be performed;

accessing, from the source address in the register file, a second operand on which the mathematical operation is to be performed;

performing the mathematical operation on the first operand and the second operand to obtain the result; and

storing the result in the destination address in the memory, wherein the destination address in the memory is different from the source address in the memory.

2. (Previously Presented) The method of claim 1, wherein the source address and the destination address in the memory correspond to 16 bit memory locations. 3.